Dose Rate Upset Investigations on the Xilinx Virtex IV Field Programmable Gate Arrays

Alonzo Vera, Daniel Llamocca, Marios Pattichis, William Kemp, Walter Shedd, David Alexander, and James Lyke

Abstract-- **The following paper describes the results of ionizing dose rate investigations into upset, supply photocurrent, latch-up, and burnout susceptibility of the Xilinx Virtex IV XC4VFX12. All investigations were performed on a commercial version of the device. The maximum no-upset dose rate was $2.8x10^8$ rad(Si)/s. Photocurrent amplitudes as a function of dose rate were recorded.**

I. INTRODUCTION

STATE-of-the-art FPGAs (field programmable gate arrays), as exemplified by the Xilinx Virtex IV family of devices, integrate a large number of system functions onto a single monolithic microcircuit.

For the XC4VFX12 devices described in this paper, the functions include: (1) 12,312 logic cells, (2) 36 block RAM/FIFO cells (each containing 18 Kbits of block SRAM), (3) four digital clock manager (DCM) blocks, (4) 32 XtremeDSPTM slices, (5) 320 programmable input/output (I/O) cells, (6) a PowerPC 405 processor block, (7) two 10/100/1000 ethernet MAC blocks, and (8) 5 Mbits of configuration memory. The diversity of resources makes this device an excellent choice for performing computational and signal processing functions in commercial systems. These capabilities are also attractive for application in aerospace systems. However, systems with radiation requirements must be cautious in including SRAM-based FPGAs due to the potential for upsetting the configuration memory, which could lead to changing the programmed functionality. Particular attention has been given to evaluating the vulnerability of high performance FPGAs to SEU (single event upsets) including effects due to heavy ions, protons, and neutrons. [1]–[5]. Although SRAM-based FPGAs are extremely vulnerable to SEU, mitigation techniques (i.e., triple modular redundancy, configuration memory scrubbing, and avoidance of half-latches) have proved to effectively enhance hardness from a functional standpoint [6]–[8].

Unfortunately, SEU mitigation techniques are not effective in hardening for an ionizing dose rate environment, which produces pervasive and simultaneous upsets throughout the circuit. The objective of the effort described in this paper was to investigate the upset, latch-up, and burn-out susceptibility of the XC4VFX12 to ionizing dose rate exposure. Evaluations were performed on a commercial version of the device, fabricated in a 90 nm technology on a silicon substrate with no epitaxial layer. The core operates at 1.2 volts, auxiliary devices operate at 2.5 volts, and the I/O may operate up to 3.3 volts.

II. TEST BOARD CONCEPT

The complexity and high performance of modern FPGAs require advanced printed circuit board design techniques to ensure that the performance advantages are preserved. Often, several versions of the boards are required to identify and optimize the operation at the board interface. Such complex development efforts are inconsistent with the resources and schedule available to a radiation test organization. An alternative approach is based on dividing the test into two efforts – (1) one directed toward upset testing and (2) the other directed toward photocurrent and latch-up characterization. Upset testing can be performed on a commercial board designed to support development and technology evaluation. The commercial board used for the upset test in this effort is shown in Fig. 1. The active support electronics are located on the board, but these components are far enough away from the Virtex IV to permit them to be shielded. The board includes its own voltage regulators to provide 1.2 volt, 2.5 volt and 3.3 volt power to the device under test. A large number of bypass capacitors are included very close to the Virtex IV to prevent voltage droop under high speed operation and to suppress noise on the supply lines. The power supply system design unfortunately also precludes easy monitoring of the photocurrent on the supply lines. It also prevents the supply current from being limited during a potential latch-up condition, making the Virtex IV susceptible to burnout if latch-up occurs. If catastrophic damage does occur, the entire board must be discarded, since the FPGA is in a ball grid array (BGA) package directly soldered to the printed circuit board. However, since the fully populated board costs less than $450 (US), the risk is

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acceptable, since a more elaborate board engineering effort would easily cost far more.

Fig. 1. Xilinx's Virtex IV FX XC4VFX12-FF668LC Development kit. For testing, the LCD panel was removed and the board was placed in a box, with lead protecting all the components but the FPGA.

Once upset testing was completed on the commercial development board, a much simpler board (Fig. 2) was designed for the sole purpose of monitoring photocurrent on the power supply lines and monitoring/limiting current during latch-up testing. Naturally, the simpler board included provisions for loading the FPGA configuration into the device under test, and monitoring its performance. However, only five CMOS output channels were made available for monitoring.

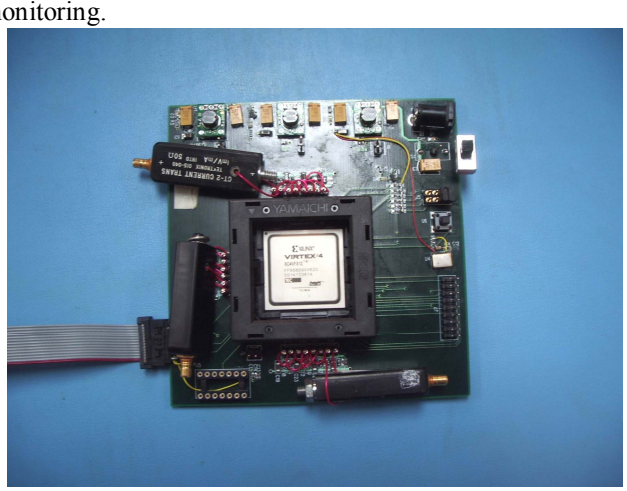

Fig. 2. Custom board design for monitoring photocurrents for the three XC4VFX12 power supplies – Vcore, Vaux, VI/O.

The photocurrent board used three Texas Instruments PTH04070WAH on-board voltage regulators driven from a common 5 volt supply to provide the three categories of supply voltage – core, aux, and I/O. The FPGA voltage pins dedicated to the specific supply voltages were connected by multiple printed wiring traces and each of the traces was bypassed by a stack of ceramic capacitors with values of 10µF, 1µF, 0.1µF, and 0.01µF. The board was designed so that a Tektronix CT-2 current probe could be inserted between the bypass capacitor stack and the FPGA voltage pins. This permitted the photocurrent for each voltage supply to be recorded independently.

The approach of separating upset testing from photocurrent characterization is a cost effective technique for radiation characterization of complex, high performance nano-scale electronics. Direct measurement of photocurrents as a function of dose rate provides system designers with the information they need to design power distribution networks to ensure that board level rail-span collapse does not compromise the upset threshold.

III. DOSE RATE UPSET PROCEDURES

The purpose of the upset test was to determine the dose rate threshold for three different photo-responses: (1) data upset, (2) configuration upset, and (3) functional interrupt/latch-up. The photo-responses were evaluated for three test configurations including: (a) a shift register configuration constructed from configurable logic block (CLB) flip flops, (b) a shift register configuration composed of a chain of 16-bit register blocks constructed from look up table (LUT) resources in each CLB, and (c) A FIFO configuration constructed from block memory.

For the two shift register configurations, the on-board 25 MHz clock was buffered out of one of the I/O ports and used to synchronize the FPGA clock with the data stream from a logic analyzer/pattern generator (Tektronix model TLA 715) as shown in Fig. 3. The shift register was tapped at four equally-spaced locations in the chain, and the output was brought out to an I/O port. The logic analyzer/pattern generator was used to monitor the outputs of the register and to generate the input pattern.

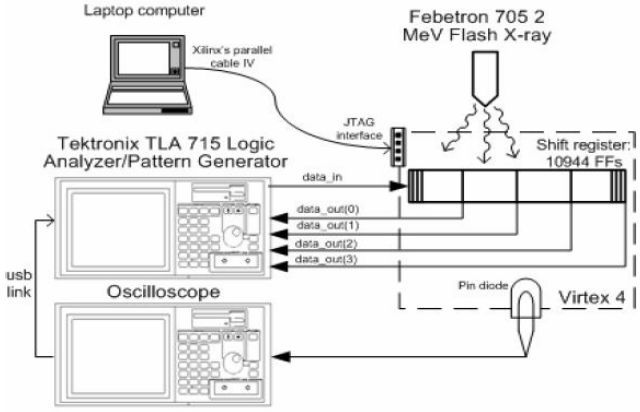

Fig. 3: Instrumentation diagram.

The Tektronix TDS-5054 oscilloscope monitored the clock output, two of the shift register outputs, and the response of the PIN diode used for secondary dosimetry. The oscilloscope was triggered by the response of the PIN diode and provided the trigger for the logic analyzer data capture so that the two instruments were synchronized.

Using both the oscilloscope and logic analyzer permitted the output of the device under test to be monitored in both the short term time regime in the vicinity of the radiation pulse and in the longer regime to detect latent upsets in the data stream or configuration. The memory depth of the logic analyzer was only sufficient to record data from one of the quadrants of the shift register for any single test. However,

there was no indication that any quadrant upset at a lower dose rate threshold than the others.

A laptop computer was used to program and verify the configuration memory of the FPGA using custom software called jtagseu [9]. The software allowed writing and reading the configuration memory at the frame level. It is similar in concept to the Xilinx FIVIT software.

For the FIFO configuration, the memory was loaded with one of three patterns from the pattern generator – all "1's", all "0's", or a logical checkerboard. An active read was initiated just prior to the radiation pulse and recorded by the oscilloscope and logic analyzer. For both the shift register and FIFO tests, the oscilloscope was configured to record 1µs around the radiation pulse and was used to determine immediate upsets in the data stream at the time of the exposure. The logic analyzer recorded the full data stream after the exposure up to its memory depth. The data stream was then checked against the expected pattern to detect any upsets that occurred in internal FPGA locations that were not immediately observable during the event.

The radiation source for all tests was the Febetron 705, 2 MeV Flash X-ray located at the Air Force Research Laboratory (AFRL), Kirtland AFB, New Mexico. Dose rates at that facility can range from below $1x10^7$ to $2x10^{11}$ rad(Si)/s by varying the distance of the device under test from the beam exit port. Dosimetry is based on CaF2 thermo-luminescent dosimeters (TLDs), which were used to calibrate a PIN diode that was located on the back of the test board. The lid was removed from one of the FPGA test articles, and three TLDs were placed in the device cavity and irradiated behind the reattached lid. The photo-charge of the PIN diode was plotted against the dose rate as determined from the average of the three TLDs. The PIN response was then used for dose rate determination for each test shot. The three TLDs exposed in the calibration shots indicated that the dose rate across the FPGA varied by no more than 5%.

IV. DOSE RATE UPSET TEST RESULTS

The upset condition was defined as a ≥33% excursion in the logic level at the time of the exposure. If no upset occurred, the device was moved closer to the FXR exit port; or if upset was detected, the device was moved farther back. The objective was to define the minimum upset and maximum no-upset dose rate threshold within a factor of two or better.

If the data stream or clock showed an upset and then returned to the correct logical operation, a data upset condition was judged to have occurred. If it did not return to the correct logical operation, a configuration upset condition was judged to have occurred. The FPGA was also examined with the jtagseu software to identify any configuration changes that were not evident in the data stream. If the device could not be reconfigured, without cycling the power supply, either a functional interrupt or latch-up was judged to have occurred. It was not possible to distinguish between a functional interrupt and a latch-up.

Fig. 4 summarizes the data and configuration upset conditions for the XC4VFX12. The lowest upset threshold was determined by upsets in the clock. A dose rate of $2.8x10^8$ rad(Si)/s was the maximum dose rate that produced no clock errors in either the CLB shift register configuration or the FIFO configuration. As shown in Fig. 5, a clock upset at a dose rate of $3x10^8$ rad(Si)/s was typical of this upset characteristic.

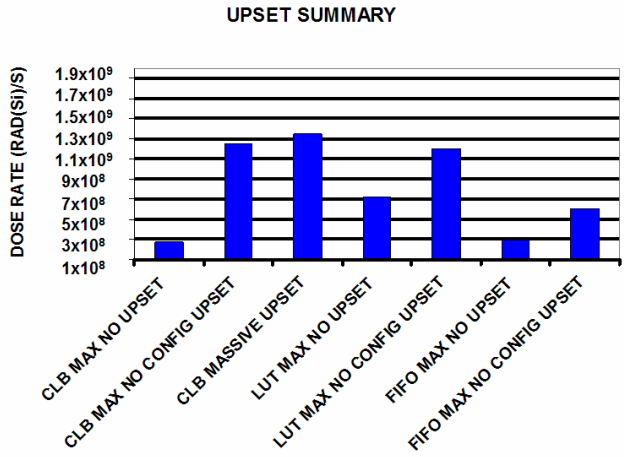

Fig. 4. Data and configuration upset summary

A latency of one clock cycle between the radiation pulse and the first clock upset was typically observed. This indicates that the upset was probably not associated with the output driver, but was most likely determined by the photo-response in the clock management unit.

Fig. 5. Clock upset in the CLB shift register configuration

As shown in Fig. 6, multiple cycle upsets in the clock produced a "stretch out" in the period of the data being cycled through the shift register. This was a further indication that the upsets were occurring in the clock distribution network and affecting the clocking of the individual flip flops in the shift register.

In all cases, the configuration upset occurred at significantly higher dose rates than the clock upset. The lowest configuration upset was observed in the FIFO. Upset occurred at $6.0x10^8$ rad(Si)/s, which was approximately a factor of 2 below the threshold of the other configurations. These upsets were typically associated with a latency in the errors observed in the data.

Fig. 6. Clock upset produces "stretch out" in data stream for CLB shift register configuration

Such a case is shown in Fig. 7, where the radiation pulse occurrence is indicated by the dashed green line and can be seen to interrupt several clock cycles. However, the data output channels recovered and appeared to be fully operational for 21 microseconds before becoming unstable. The FPGA was found to have 1556 configuration errors when it was examined after the test.

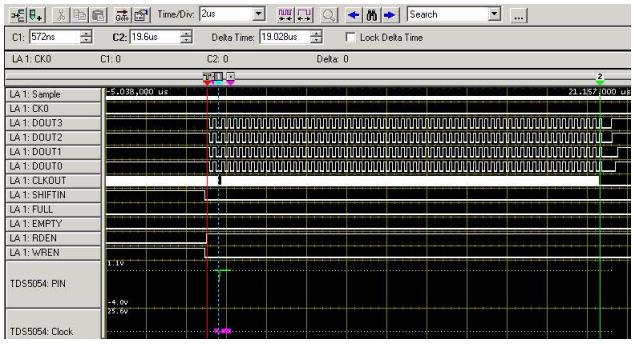

Fig. 7. Data upset latency in a FIFO configuration with multiple configuration errors

In addition to the upset testing, a limited set of higher dose rate tests were also conducted. The mechanical arrangement limited the dose rate to 9×10^9 rad(Si)/s and the tests were conducted at room temperature. Of the two devices tested on the MEMEC board, one device entered a non-responsive state following the radiation pulse. The device could not be reconfigured without recycling the power. The state could have been either a functional interrupt or a latch-up. There was no capability to distinguish between the two conditions. The device was fully functional after the power supply recycling.

V. PHOTOCURRENT RESULTS

The photocurrent monitoring board was used to test two FPGAs to determine photocurrent as a function of dose rate. Supply photocurrent was recorded for each of the three supplies. Dose rates ranged between 3.4×10^7 and 6.2×10^9 rad(Si)/s. The results for each of the power supply types are shown in Fig. 8. As might be expected the photocurrent of the core supply was dominant. The auxiliary and I/O showed significantly less photocurrent. However, only five of the CMOS I/Os were used and the remainder were unconfigured. Similarly, none of the circuitry served by the auxiliary supply was configured. Their response may have been greater for an actual application. The core was configured for a CLB shift register. Linear equations were fit to each of the data sets and the resulting curves are plotted in Fig. 8. The fits were made to the low dose rate data ($<10^8$ rad(Si)/s) and extrapolated to the higher dose rates.

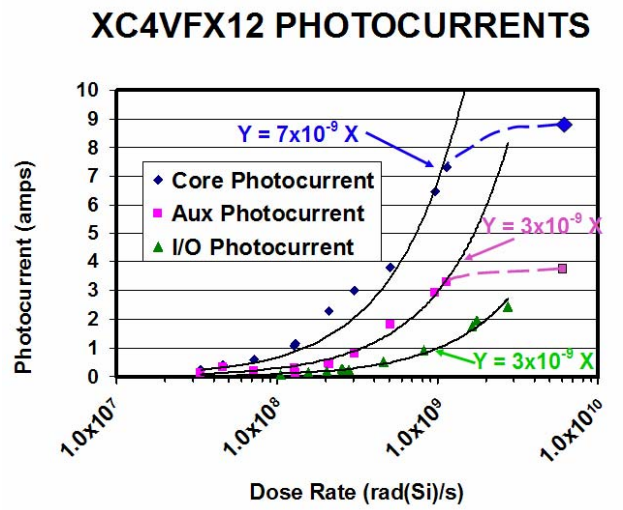

Fig. 8. Photocurrents for the three voltage supply types used in the V4 FPGA

For the core supply, the photocurrent trends super-linear beginning around 10^8 rad(Si)/s, possibly indicating the turn-on of parasitic bipolar devices associated with the well and substrate. At dose rates above 10^9 rad(Si)/s the currents begin to saturate with a maximum peak value of 8.8 amps. The printed circuit board trace resistance of the power supply network may have contributed to the photocurrent saturation.

After each photocurrent test, the configuration of the FPGA was monitored. For this series of tests, the configuration was lost at dose rates as low as 7×10^7 rad(Si)/s. Most likely, this was caused by the lack of bypass capacitance very close to the supply pins.

One of the devices in this series of tests also entered a non-responsive state at dose rates as low as 6×10^9 rad(Si)/s. The response was repeatable and occurred every time the dose rate exceeded that threshold. The device could not be reconfigured without cycling the power supply. The photocurrent waveform shown in Fig. 9 has a very long recovery time which is probably not accurately followed by the CT-2 current probe due to amp*second product limitations. The dc current to the part increased from 174 mA pre-irradiation to 300 mA after the pulse. The current was stable at that value until the supply was recycled.

VI. SUMMARY

The dose rate evaluations of the Xilinx Virtex IV XC4VFX12 indicated a maximum no-upset threshold of 2.8×10^8 rad(Si)/s based on a well designed commercial printed circuit card. The minimum upset threshold appeared to be associated with the clock distribution network.

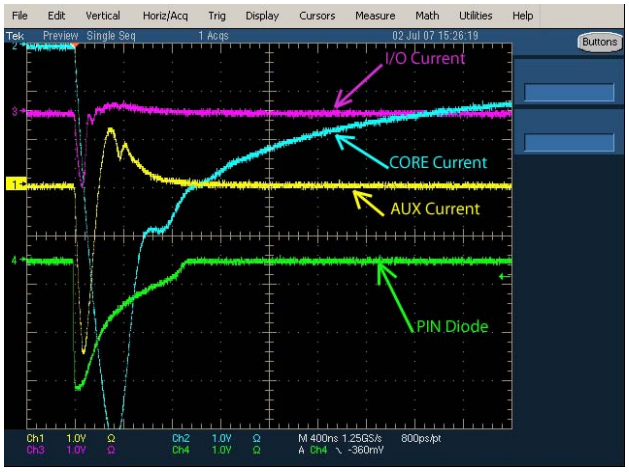

Fig. 9. Photocurrent response for non-responsive state

Photocurrent measurements indicated some super-linearity of response beginning around 1.0×10^8 rad(Si)/s, which was consistent with the measured upset threshold. Non-responsive states were observed in both the upset and photocurrent testing. The non-responsive state could have been either a latch-up or a functional interrupt. No permanent degradation of the part was observed after any of the testing.

VII. References

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